Notice of Allowability	Application No.	Applicant(s)	
	10/623,099	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the interview on 09/19/06 and the communication fied on 07/17/2006*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DIEU-MINH LE
PRIMARY EXAMINER

1. This office action is in response to the Interview on 09/19/2006 and the communication filed 07/17/2006.

2. Claims 1-21 are allowable over the prior art of record.

3. An Examiner's Amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 C.F.R. § 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the Issue Fee.

EXAMINER'S AMENDMENT:

IN THE CLAIMS:

Please replace all prior versions of claims in the application with the current listing claims in the **ATTACHMENT:**

4. Authorization for this Examiner's Amendment was given in a telephone interview with Mr. James K. Okamoto, Registration No. 40,110 on 09/19/2006.

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably **accompany** the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

DML.
09/21/2006

ATTACHMENT:

LISTING OF CLAIMS:

1. (currently amended) A single central processing unit (CPU) for targeted fault-tolerant computing , the CPU comprising:
   decode circuitry in the single CPU configured to decode a fault-tolerant version of an instruction and a non-fault-tolerant version of the instruction distinctly from each other; and
   execution circuitry in the single CPU configured to execute the fault-tolerant version of the instruction with redundancy checking and to execute the non-fault-tolerant version of the instruction without redundancy checking.

2. (previously presented) The CPU of claim 1, wherein the execution circuitry includes:
   a first processing unit configured to receive operand data, execute an operation associated with the instruction; and generate a first result;
   a second processing unit configured to receive the operand data; execute the operation, and generate a second result;
   a comparator configured to compare the first and second results.

3. (previously presented) The CPU of claim 2, wherein for the fault-tolerant version of the instruction, if the comparison does not match, then repeating the execution by the processing units and the comparison of results by the comparator up to a maximum N times until a match occurs.

4. (previously presented) The CPU of claim 3, wherein, if the first and second results never match, a machine check is performed on the microprocessor.

5. (previously presented) The CPU of claim 2, further comprising:
a register file configured to provide both the first and second processing units with the operand data.

6. (currently amended) A method for targeted fault-tolerant computing in a single central processing unit (CPU), the method comprising:
decoding a first op code in the single CPU corresponding to a fault-tolerant version of an instruction;
decoding a second op code in the single CPU corresponding to a non-fault-tolerant version of the instruction;
executing the first op code in the single CPU with redundancy checking; and
executing the second op code in the single CPU without redundancy checking.

7. (original) The method of claim 6, wherein a set of multiple instructions is provided in fault-tolerant and non-fault-tolerant versions of each instruction in the set.

8. (original) The method of claim 7, wherein the set of instructions includes arithmetic functions.

9. (original) The method of claim 7, wherein the set of instructions includes logical functions.

10. (original) The method of claim 6, wherein the execution of first op code comprises:
providing operand data to a first processing unit;
providing the operand data to a second processing unit;
executing an operation on the operand data by the first processing unit to generate a first result;
executing the operation on the operand data by the second processing unit to generate a second result; and
comparing the first and second results.

11. (original) The method of claim 10, further comprising, if the first and second results do not match, repeating the execution and comparison steps.

12. (original) The method of claim 11, wherein the repeating continues up to a maximum of N times until the first and second results match.

13. (original) The method of claim 12, further comprising, if the first and second results never matched during the N repetitions, performance of a machine check on the CPU.

14. (currently amended) A ~~computing apparatus~~ single microprocessor for targeted fault-tolerant computing, the ~~apparatus~~ microprocessor comprising:
means in the microprocessor for decoding a first op code corresponding to a fault-tolerant version of an instruction and a second op code corresponding to a non-fault-tolerant version of the instruction;
redundant means in the microprocessor for executing the first op code; and
non-redundant means in the microprocessor for executing the second op code.

15. (currently amended) The ~~apparatus~~ microprocessor of claim 14, wherein the redundant means comprises:
a first processing unit configured to receive operand data, execute an operation associated with the first op code; and generate a first result;
a second processing unit configured to receive the operand data; execute the operation, and generate a second result;
a comparator configured to compare the first and second results.

16. (currently amended) A computer program product comprising a computer-usable medium having computer-readable code embodied therein for execution on a single microprocessor having decode and execution circuitry for decoding and

executing fault-tolerant versions of instructions with redundancy checking and for decoding and executing non-fault-tolerant versions of instructions without redundancy checking, the computer program product including:

a first type of computer-readable instructions comprising fault-tolerant instructions to be executed with redundancy checking; and

a second type of computer-readable instructions comprising non-fault-tolerant instructions to be executed non-redundantly.

17. (original) The computer program product of claim 16, wherein the first type of computer-readable instructions includes fault-tolerant arithmetic instructions.

18. (original) The computer program product of claim 17, wherein the second type of computer-readable instructions includes non-fault-tolerant arithmetic instructions.

19. (original) The computer program product of claim 16, wherein the first type of computer-readable instructions includes fault-tolerant logical functions

20. (original) The computer program product of claim 19, wherein the second type of computer-readable instructions includes non-fault-tolerant logical instructions.

21. (original) The method of claim 11, further comprising, if the first and second results do not match, logging a comparison error.